£1.5 million available to experiment on CHERI architecture within defence and security systems

- DASA has launched a new Themed Competition: CHERI within Defence and Security
- Funded by Defence Science and Technology Laboratory (Dstl) Cyber Programme
- £1.5 million funding available to experiment and trial the effects of the CHERI (Capability Hardware Enhanced RISC Instructions) based architecture extensions within the Arm's Morello prototype System on Chip (SoC)

The Defence and Security Accelerator (DASA) is pleased to launch a new Themed Competition, CHERI within Defence and Security. Run on behalf of the Defence Science and Technology Laboratory (Dstl) Cyber Programme, this competition seeks proposals to experiment and trial the effects of the CHERI (Capability Hardware Enhanced RISC Instructions) based architecture extensions within Arm's Morello prototype System on Chip (SoC) for defence and security.

Key dates and funding

£1.5 million funding is available for this Themed Competition, and we expect to fund several proposals up to £100k.

The deadline to submit a proposal is midday 14 November 2022

Do you have a useful idea for testing CHERI within Defence and Security? Read the full competition document and submit a proposal.

What is Arm Morello and CHERI?

Cyber security needs to keep pace with the rapid evolution of technologies, and currently, a lot of time, effort and money is spent on patching systems so they are more secure. However, in a world with uncertain technological and military challenges, systems that are built from the ground up to be more resilient to attacks is vital for a safer future.

The Arm Morello Program, funded by Digital Security by Design (DSbD), is a collaboration between academia, industry and government to research and create more secure hardware and software to improve built-in security. CHERI (Capability Hardware Enhanced RISC Instructions) is the key underpinning technology that addresses memory safety issues and enables fine grain protection of applications.

Using this technology, Arm has designed a prototype SoC and development board, called the Morello board, the world's first industrial quality implementation of CHERI. The Morello board is being distributed to industry

and academia to test the prototype architecture to investigate and experiment on its capabilities.

Evaluating CHERI within Defence and Security

The CHERI within Defence and Security Themed Competition is aimed at providing the Morello board to the Defence and Security sector for research, evaluation and experimentation. Successful proposals will be provided with the Morello board to trial and evaluate the effect of the new technologies within their defence systems.

Challenge areas

The competition has three challenge areas. Proposals may address more than one challenge.

Code Porting

This challenge area seeks to port an existing codebase or tool (e.g. compiler) into the Morello environment and strengthen its security by using the Morello enhanced security features.

Software Compartmentalisation

This challenge area seeks to refactor an existing application to employ fine grain software compartmentalisation.

Innovation

This challenge area seeks to conduct research in an area in line with competition scope, such as a security enhancing innovation, now enabled by the availability of the Morello features.

To learn more about the challenge areas of the competition, read the full competition document.

Submit a proposal

Do you have an innovative project to test the CHERI based architecture in a defence setting? Submit your idea and help create a safer and more cyber resilient defence.

Learn more and submit a proposal.